PATENT ABSTRACTS OF JAPAN

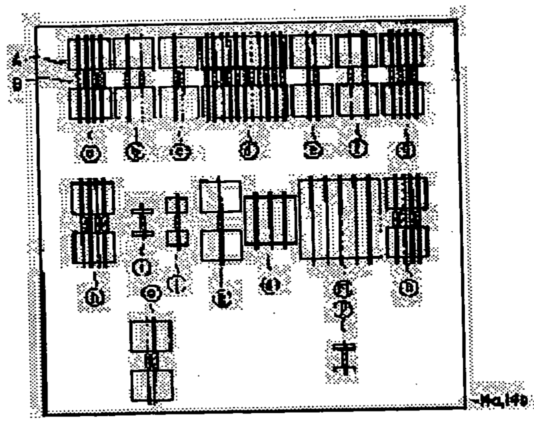
(11)Publication number : 10-050785
(43)Date of publication of application : 20.02.1998

(51)Int.Cl. H01L 21/66

(21)Application number : 08-199058
(22)Date of filing : 29.07.1996
(71)Applicant : TOSHIBA CORP
(72)Inventor : HATANAKA KAZUHISA

(54) MONITOR PATTERN

(57)Abstract:
PROBLEM TO BE SOLVED: To monitor dispersion in dimension of all of device formation patterns by forming monitor patterns having a plurality of step patterns so as to reproduce a step in an underlayer of a device formation pattern.
SOLUTION: Monitor patterns 14a and 14b are formed by unit patterns a to p. Each of the unit patterns a to p is constructed by a rectangular SDG region pattern (low stepped pattern) A and a linear gate wiring pattern (resist film pattern) B as a target to be monitored. For example, unit patterns a, g, h, and n are formed so that the interval between two SDG region patterns A most occupying the area in an actual LSI is minimized on the layout. The gate wiring patterns B each having the narrowest gate width permitted on the design rule are formed at the narrowest spacing on the underlayer steps including the two SDG region patterns A.



LEGAL STATUS

[Date of request for examination]	02.03.2000
[Date of sending the examiner's decision of rejection]	12.02.2003
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

Translation of [0012]-[0045] in the Description of H10-50785

[0012]

[Embodiment of the Invention] There will now be described embodiments of this invention with reference to the accompanying drawings. The FIG. 1 is an outline configuration showing a semiconductor wafer in which desired semiconductor integrated circuit devices (LSI devices) are formed. The (a) of the figure is a plan view showing a substantial part of the semiconductor wafer, and the (b) in the figure is an enlarged view of a monitor pattern forming area shown to be taken out of it.

[0013] A semiconductor wafer (semiconductor substrate) 11 is divided into a plurality of element formation areas 13 in which LSI devices are formed by scribe lines 12.

[0014] On the scribe lines 12, monitor pattern formation regions 14 are formed corresponding to the respective element formation areas 13. In each of the monitor pattern formation regions 14, one set (one pair) of monitor patterns 14a, 14b are formed.

[0015] The monitor patterns 14a, 14b above are arranged with the directions thereof set at an angle of 90 DEG. The FIG. 2 is a plan view showing one example of the above monitor patterns 14a, 14b in one embodiment of the present invention.

[0016] The monitor patterns 14a, 14b are used for monitoring a variation in the patterning dimension of the gate wiring in the actual LSI device and are constructed by 16 unit patterns a to p. Each of the unit patterns a to p includes a rectangular SDG region pattern (low step pattern) or patterns A and a linear gate wiring pattern (resist film pattern) or patterns B to be monitored.

[0017] In each of the unit patterns a, g, h and n in the monitor

patterns 14a, 14b, two SDG region patterns A, each having an area equal to one of areas which is provided in largest numbers in the actual LSI device, are arranged at the shortest interval on the layout. Further, four gate wiring patterns B having the gate dimension of minimum permissible width on the design rule (the minimum gate dimension which determines the operation speed of the LSI device), are formed at the shortest interval among the intervals on the background stepped portion containing the two SDG region patterns A.

[0018] For example, in each of the unit patterns b and f, two SDG region patterns A, each having an area equal to one of the areas which is provided in largest numbers in the actual LSI device, are arranged at the shortest interval on the layout. Further, two gate wiring patterns B having the gate dimension of minimum permissible width on the design rule, are formed at the largest interval among the intervals on the background stepped portion containing the two SDG region patterns A.

[0019] For example, in each of the unit patterns c, e and o, two SDG region patterns A each having an area equal to one of the areas which are provided in largest numbers in the actual LSI device are arranged at the shortest interval on the layout. Further, two gate wiring patterns B having the gate dimension of minimum permissible width on the design rule, are formed at the shortest interval among the intervals on the background stepped portion containing the two SDG region patterns A.

[0020] For example, in the unit pattern d, two SDG region patterns A, each having an area which is larger than each of the areas which are provided in largest numbers in the actual LSI device, are arranged at the shortest interval on the layout. Further,

eleven gate wiring patterns B having the gate dimension of minimum permissible width on the design rule are formed at the shortest interval among the intervals on the background stepped portion containing the two SDG region patterns A.

[0021] For example, in each of the unit patterns i and p, two SDG region patterns A, each having a minimum permissible area on the design rule, are arranged at the shortest interval on the layout. Further, one gate wiring pattern B having the gate dimension of minimum permissible width on the design rule is formed on the background stepped portion containing the two SDG region patterns A.

[0022] For example, in the unit pattern j, two SDG region patterns A, each having an area which is a little larger than the minimum permissible area on the design rule, are arranged at the shortest interval on the layout. Further, one gate wiring pattern B having the gate dimension of minimum permissible width on the design rule is formed on the background stepped portion containing the two SDG region patterns A.

[0023]

For example, in the unit pattern k, two SDG region patterns A, each having an area equal to one of the areas which is provided in largest numbers in the actual LSI device, are arranged at the shortest interval on the layout. Further, one gate wiring pattern B having the gate dimension of minimum permissible width on the design rule is formed on the background stepped portion containing the two SDG region patterns A.

[0024] For example, in the unit pattern l, one SDG region pattern A having an area which is a little larger than each of the areas which are provided in largest numbers in the actual LSI device

is formed. Further, three gate wiring patterns B having the gate dimension of minimum permissible width on the design rule are formed at the largest interval among the intervals on the background stepped portion containing the SDG region pattern A.

[0025] For example, in the unit pattern m, one SDG region pattern A having an area in which the film thickness of a resist film is saturated in the actual LSI device is formed. Further, five gate wiring patterns B, each having the gate dimension of minimum permissible width on the design rule, are formed at the largest interval among the intervals on the background stepped portion containing the SDG region pattern A.

[0026] The unit patterns a to n are patterns which are densely formed close to each other. The unit patterns o and p are patterns which are respectively obtained by independently and sparsely forming the unit pattern c, e and the unit pattern i which are arranged in a dense form.

[0027] According to the monitor patterns 14a, 14b, for example, a variation in the patterning dimension of the gate wiring caused by a difference in the area of the SDG region on the actual LSI device can be monitored based on a difference (variation) in the patterning dimension of each of the gate wiring patterns B of the unit patterns i to m.

[0028] Further, for example, a variation in the patterning dimension of the gate wiring depending on a difference in the density (dense or sparse arrangement) of the gate wirings on the actual LSI device can be monitored based on a difference in the patterning dimension of each of the gate wiring patterns B of the unit patterns a to c and k.

[0029] Further, for example, a variation in the patterning

dimension of the gate wiring depending on a difference in the density (dense or sparse arrangement) of the SDG regions on the actual LSI device can be monitored based on a difference in the patterning dimension of each of the gate wiring patterns B of the unit patterns c and o and the unit patterns i and p.

[0030] Further, for example, a variation in the patterning dimension of the gate wiring caused by the proximity effect on the actual LSI device can be monitored based on a difference in the patterning dimension of each of the gate wiring patterns B of the unit pattern d.

[0031] Thus, for example, if the monitor pattern 14a is formed based on the relation between the area of the background SDG region and the film thickness of the resist film, the relation between the dense/sparse arrangement of the SDG region and the film thickness of the resist film, and the dense/sparse arrangement of the gate wiring in the actual LSI device, the etching conversion difference derived by use of the monitor pattern 14a can be applied to all of the gate wirings in the LSI device and it becomes possible to monitor variations including a variation in the patterning dimension of the gate wiring in the actual LSI device.

[0032] That is, in the monitor pattern 14a, the film thickness of the resist film which varies depending on a difference in the area of the SDG regions randomly arranged on the actual LSI device can be realized by changing the area of the SDG region pattern A, for example, from the minimum area which can be attained on the design rule to the maximum area in which the film thickness of the resist film is saturated.

[0033] Further, in the monitor pattern 14a, the film thickness of the resist film which varies depending on a difference in the

density of arrangement of the SDG regions randomly arranged on the actual LSI device can be realized by changing the density of arrangement of the SDG region patterns A, for example, from the highest density thereof which can be attained on the layout to substantially the lowest density thereof.

[0034] Further, in the monitor pattern 14a, the microloading effect caused by a difference in the density of arrangement of the gate wirings on the actual LSI device can be artificially realized by changing the arrangement interval of the gate wiring patterns B, for example, from the minimum interval at which they are arranged with the highest permissible density on the layout to the maximum interval at which they are arranged with substantially the lowest density.

[0035] Further, in the monitor pattern 14a, the proximity effect caused by the dense arrangement of the gate wirings on the actual LSI device can be artificially realized by arranging the gate wiring patterns B as close to each other as possible on the layout.

[0036] Since the monitor pattern 14b which is obtained by rotating the monitor pattern 14a by 90 DEG is provided together with the monitor pattern 14a, a variation in the patterning dimension of the gate wiring due to the microloading effect on the actual LSI device, which is caused by a difference in the patterning dimension of the gate wiring pattern B due to a difference in the direction in which liquid developer flows, can be monitored.

[0037] The FIG. 3 shows the correlation between the area of the background SDG region and the film thickness of the resist film in an LSI device. Since the film thickness of the resist film also depends on the area of the background SDG region, the areas of the SDG region patterns A in the unit patterns a to p of the

monitor patterns 14a, 14b are determined based on the above correlation, for example.

[0038] Thus, the area of the SDG region pattern A in the unit pattern m having the maximum area in which the film thickness of the resist film is saturated can be derived with high precision. The FIG. 4 is a histogram for verifying the monitoring performance realized by use of the monitor patterns 14a, 14b. The (a) of the figure shows the result of evaluation of a variation in the patterning dimension of the gate wiring pattern B in the monitor pattern 14a, 14b for an LSI device by using an actual product and the (b) of the figure shows the result of evaluation of a variation in the actual patterning dimension of a typical gate wiring in the above LSI device by using the actual product.

[0039] As is clearly understood from this figures, for example, a variation in the patterning dimension of the gate wiring pattern B in the monitor pattern 14a completely covers (contains) a variation in the patterning dimension of the gate wiring in the actual LSI device.

[0040] Therefore, it is possible to strictly ensure the precise finish dimension of the gate wiring in the LSI device by monitoring whether the dimension of the gate wiring pattern B of the monitor pattern 14a lies within the specification limit.

[0041] Further, if it is detected by the monitoring that the finish dimension of the gate wiring in the LSI device lies outside the allowed specification limit, the off-specification gate wiring pattern B is specified and the dependency on the cause of the variation in the patterning dimension is determined so that the cause of the variation can be easily estimated and the countermeasure and evaluation can be made in the early stage.

[0042] As described above, a variation in the patterning dimension of the gate wiring on the actual LSI device can be completely covered. That is, the monitor pattern is formed based, for example, on the relation between the area of the background SDG region and the film thickness of the resist film, on the relation between the dense/sparse arrangement of the SDG region and the film thickness of the resist film, and on the dense/sparse arrangement of the gate wiring in the actual LSI device. Therefore, the etching conversion difference derived by use of the monitor pattern can be applied to all of the gate wirings in the LSI device. Thus, it becomes possible to monitor variations including a variation in the patterning dimension of the gate wiring in the actual LSI device and more strictly ensure the precise finish dimension of the LSI device.

[0043] In the embodiment of this invention described above, a case wherein the monitor pattern is formed on the scribe line is explained, but this is not limiting. For example, it is possible to form it in a space area of the element formation area.

[0044] Further, this invention can be applied not only to a case wherein a variation in the patterning dimension of the gate wiring is monitored, but also to a case wherein a variation in the patterning dimension of an upper wiring of a multilayer wiring structure is monitored, for example. In addition, it is of course possible to variously modify this invention without departing from the technical scope thereof.

[0045]

[Effect of the Invention] As described above, according to this invention, a monitor pattern can be provided with which variations in the dimensions of all of the element forming patterns in an

actual semiconductor integrated circuit device can be monitored and in which the precise finish dimension of the semiconductor integrated circuit device can be strictly ensured.

[BRIEF DESCRIPTION OF THE DRAWING]

[FIG. 1] It is an outline constitution view showing a semiconductor wafer in which LSI devices are formed.

[FIG. 2] It is an outline constitution view showing a monitor pattern on one embodiment of this invention.

[FIG. 3] It is a diagram showing the correlation between the area of an SDG region which is a background and the film thickness of a resist film in one LSI device.

[FIG. 4] It is a diagram showing the monitoring performance of a monitor pattern.

[Description of the signs]

11 … a semiconductor wafer;

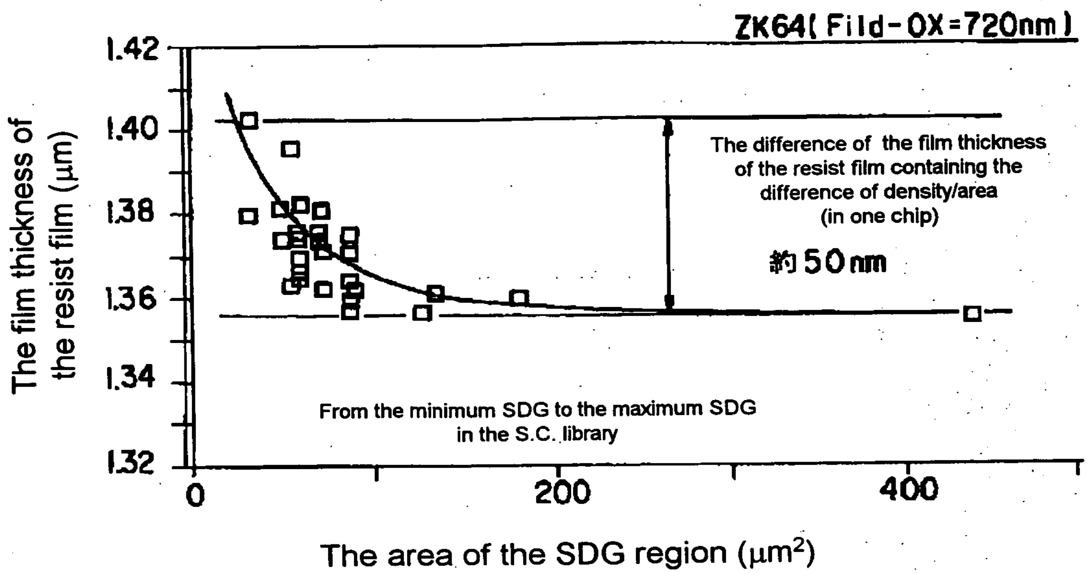
12 … scribe lines;

13 … element formation areas;

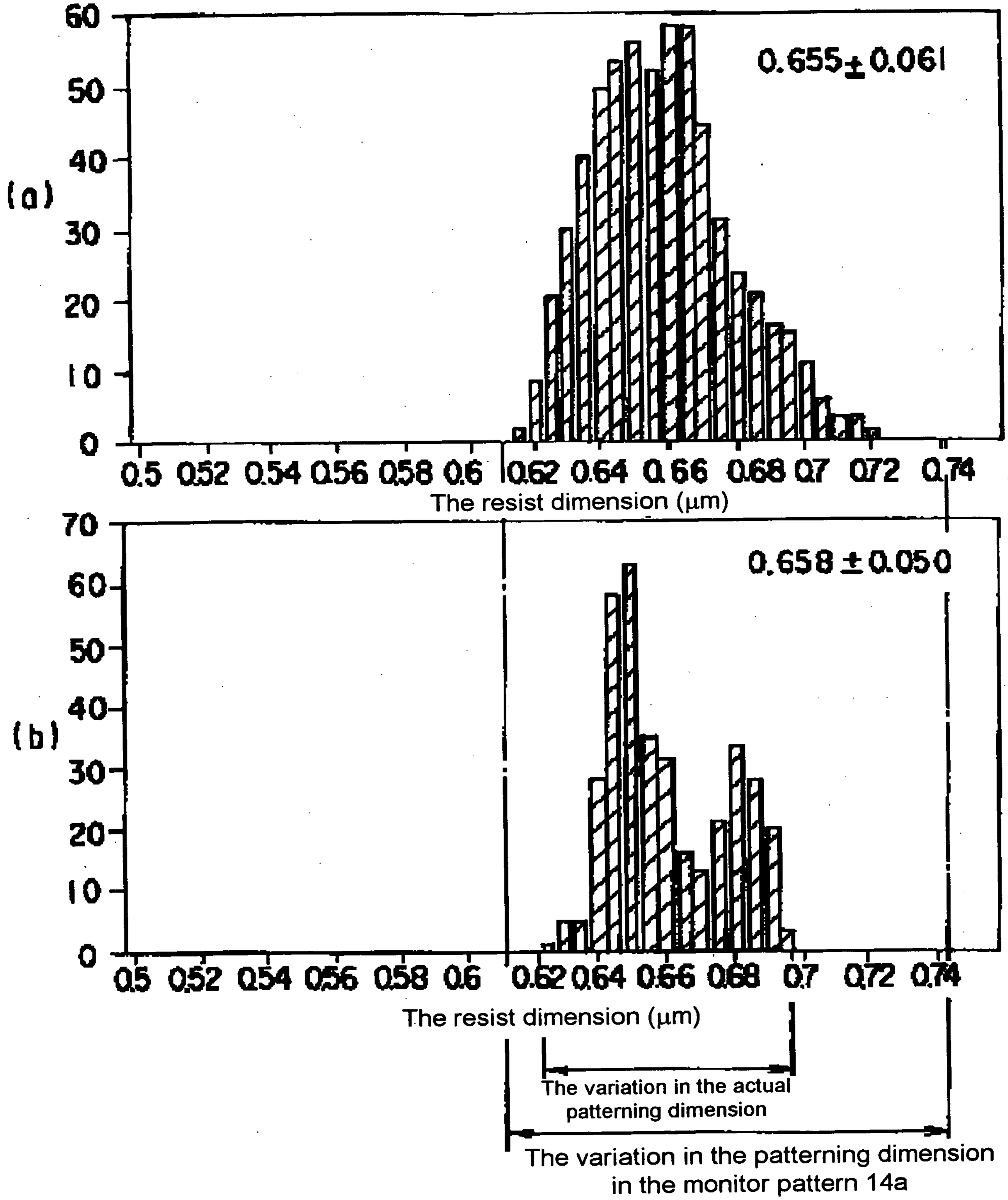
14 … a monitor pattern formation region;

14a, 14b … monitor patters.

【FIG.3】


ZK64(Fild-OX=720nm)
1.42
1.40
1.38
1.36
1.34
1.32
The film thickness of the resist film (μm)
The difference of the film thickness of the resist film containing the difference of density/area (in one chip)
約50nm
From the minimum SDG to the maximum SDG in the S.C. library
0
200
400
The area of the SDG region (μm2)

【FIG.4】


(a)
60
50
40
30
20
10
0
0.655±0.061
0.5 0.52 0.54 0.56 0.58 0.6 0.62 0.64 0.66 0.68 0.7 0.72 0.74
The resist dimension (μm)
(b)
70
60
50
40
30
20
10
0
0.658±0.050
0.5 0.52 0.54 0.56 0.58 0.6 0.62 0.64 0.66 0.68 0.7 0.72 0.74
The resist dimension (μm)
The variation in the actual patterning dimension
The variation in the patterning dimension in the monitor pattern 14a